

Fundamentals of Microcontroller

SOLUTION TO PROBLEMS

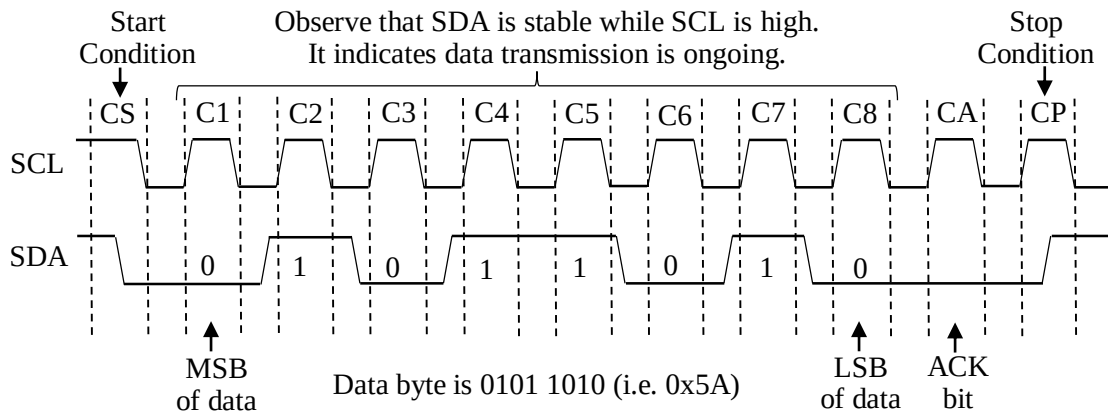
- 13.1** In MCS 51 family MCU 8031 has no in-built ROM. 8051 has ROM, 8751 is UV-EPROM, 89C51 is EEPROM.
- 13.2** Usually timers in MCU can be 8-, 16- or 32-bits and they can operate in one-time or auto-reload mode.
- 13.3** While selecting a MCU with on chip DAC one has to look for specifications like sampling rate, Dynamic range, Interface type, Resolution, current sinking and sourcing capacity etc.
- 13.4** While selecting a MCU with on chip ADC one has to look for specifications like sampling rate, Resolution required, Quantization error, Reference Voltage range, Analog Input Voltage range, Resolution required, Quantization error etc.
- 13.5** A watchdog timer (WDT) designed to generate reset pulses periodically. Under normal scenario the system software reset WDT before it generates reset pulse. However, when a fault occurs, the system software hangs and it cannot kick the dog. As a result, time (pre-determined) to deactivate the WDT lapses and the WTD generates reset pulse. Thus, MCU will reboot and one can regain control of the system.
- 13.6** Comparison between I²C and SPI protocol

I ² C Protocol	SPI Protocol
Two wires are required.	Minimum four wires are required.
It is a half-duplex protocol.	It is a full duplex protocol.
There can be multiple masters in the system.	Only single-master system.
Pull up resistors are a must.	Pull up resistors are not required.

- 13.7** Two types of SPI device configurations are —independent slave configuration and daisy chain configuration. If each slave device has a separate chip select signal, it is called as independent slave configuration. It means, master device must have chip select pins equal to number of slave devices to be interfaced in addition to basic 4-wire interface signals, as shown in Fig. 13.3(a). This increases the number of connections to be made in a system. In daisy chain configuration, only one chip select is required for all the slaves, as shown in Fig. 13.3(b). However, the data bytes propagate from one slave to other and hence overall system performance deteriorate.
- 13.8** There are five operating speed categories in I²C which are as follows:
- Bidirectional bus
 - Standard-mode (Sm), with a bit rate up to 100 kbit/s
 - Fast-mode (Fm), with a bit rate up to 400 kbit/s
 - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s

- High-speed mode (Hs-mode), with a bit rate up to 3.4 Mbit/s
- Unidirectional bus
- Ultra Fast-mode (UFm), with a bit rate up to 5 Mbit/s

13.9 Waveforms representing successful transfer of data byte 0x5A using I²C protocol.



13.10 Waveforms representing successful transfer of data byte 0xCD using I²C protocol.

